**ECEN3017 ANALOG INTEGRATED CIRCUIT DESIGN Spring 2021**

**Project Tutorial 1a: Schematic Design in Cadence**

**Objectives**

To get yourself familiarized with the EDA tool Cadence/Spectre (which is a powerful circuit schematic/layout entry and simulation tool) by designing a common source (CS) amplifier. The objectives of this project tutorial include: (1) construct and simulate some basic performance parameters of a CS amplifier in Spectre; (2) study to layout the circuits using Virtuoso/Calibre with Design Rule Check (DRC), Layout Versus Schematic (LVS) and Post-Layout Simulated (PLS) passed. Tutorial 1a will focus on the discussion of objective (1).

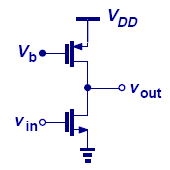
**Design Specifications**

Supply voltage: 1.2V

Technology: ST 65nm process

Loading capacitance: 1pF

|  |  |
| --- | --- |
|  | Common Source |
| Gain | >20 dB |
| GBW | >400 MHz |
| Power consumption | <1 mW |

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**Cadence IC Design Flow**

**Circuit Design**

**Circuit Schematic Design**

(Virtuoso schematic composer)

**Circuit Simulation**

(Analog Design Environment)

**Layout Design**

(Virtuoso Layout Editing)

**Layout Design Rule Check**

**(DRC)**

(Calibre)

**Layout Versus Schematic (LVS)**

(Calibre)

**Parasitic Extraction (PE)**

(Post-Layout Simulation)

**Post-Layout Simulation**

(Analog Design

Environment)

**Final Layout File**

(GDS II)

**Tutorial Contents**

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6. Add Wire Name

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2. Edit Component’s Properties
3. Check and Save

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2. Create Symbol
3. Update Symbol
4. Build Test-Bench

Test-bench Editing

1. Modify Schematic in Test-Bench
2. Run simulation

Simulation

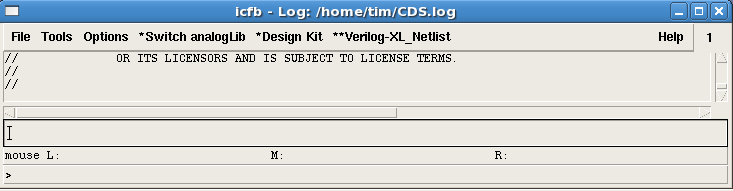
1. Check results
2. Exit Cadence
3. Appendix

**I. Access Cadence**

***Note: You can refer the Appendix for some useful hot-keys to help you with your schematic entry.***

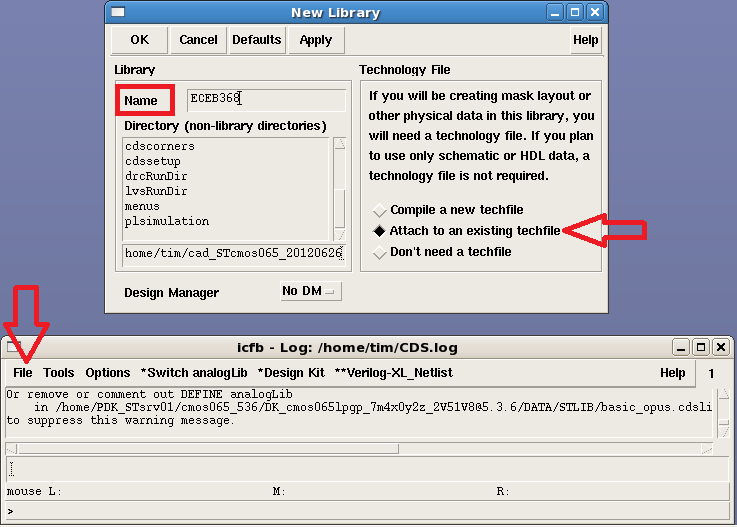
Remote access to VLSI lab’s computer and start-up Cadence with a remote terminal. *(Follow* ***the instructions*** *given on the class)*

If successful, you will see the **icfb** window:

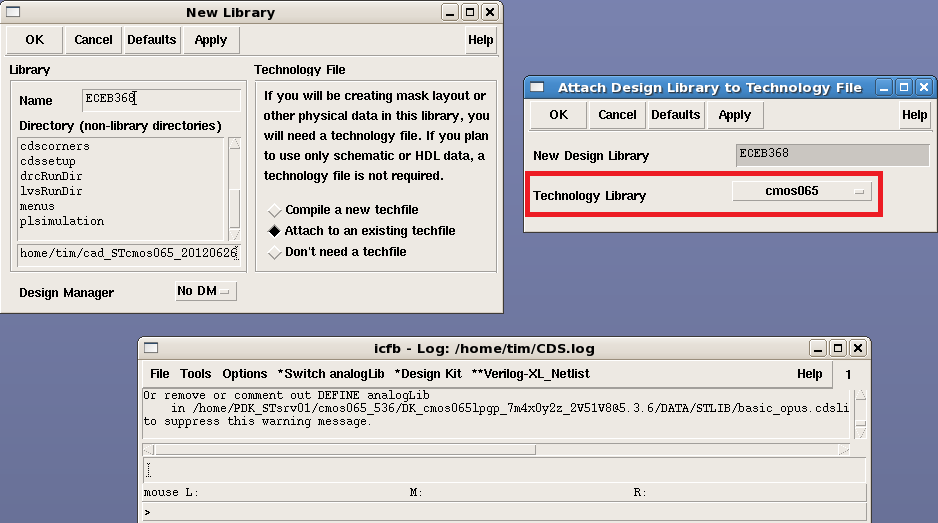


**II. Create New library**

1. On the **icfb** interface: **File** -> **New** -> **Library**
2. Type in the library name (e.g. ECEB368)
3. Select “**Attach to an existing techfile”,** -> press OK.

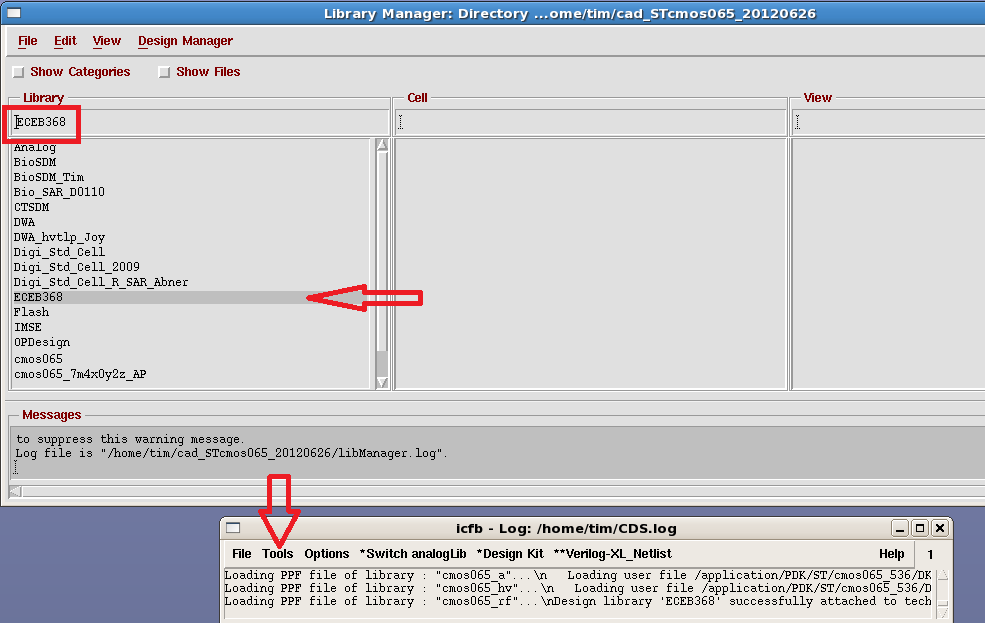


1. In the appeared window, under **Technology Library**, select “**cmos065”**, and press **OK**.

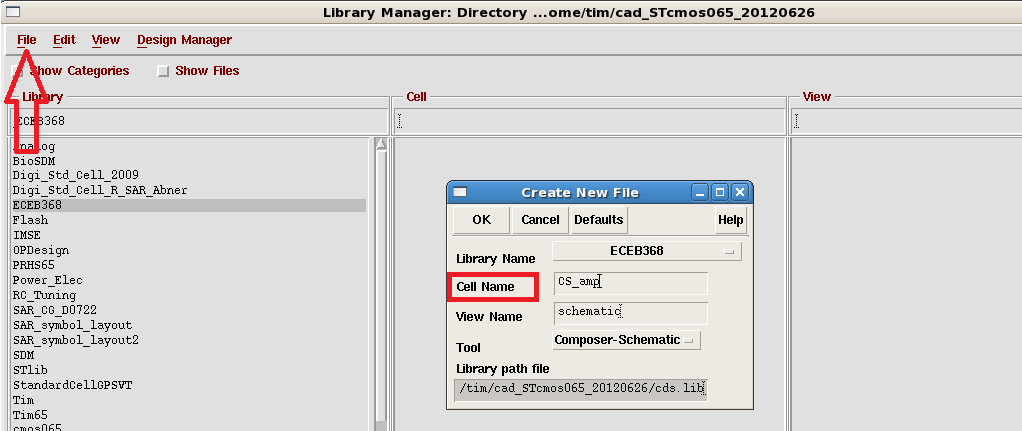


**III. Create New Schematic**

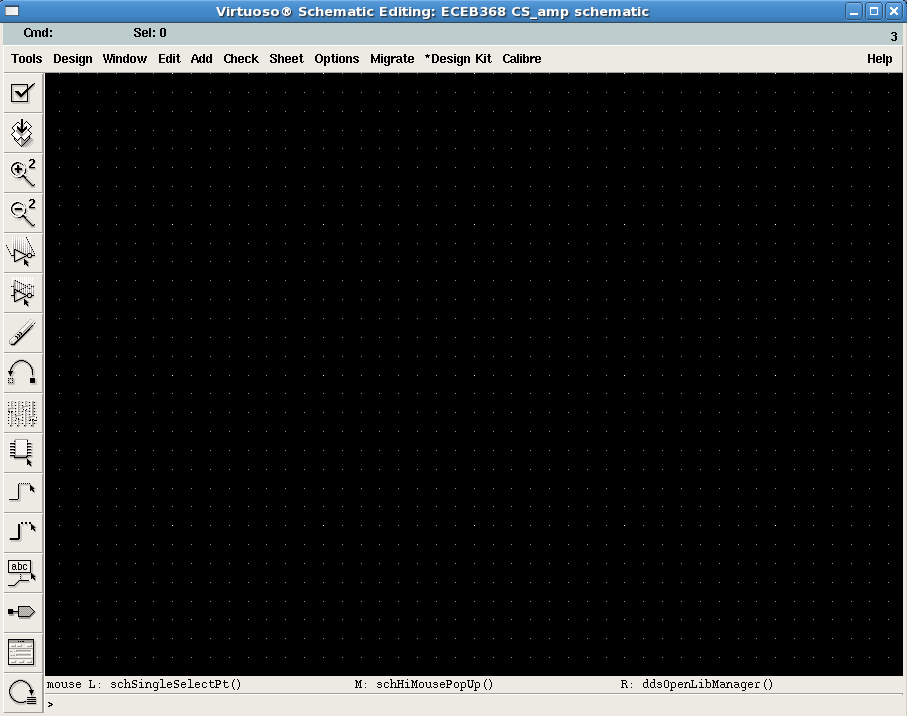
1. Open **Library Manager**: on **icfb** -> **Tools** -> **Library Manager**
2. Select the created library **ECEB368** from the list.



1. Select **File** -> **New** -> **Cell View**
2. Type in the **Cell Name** (e.g. CS\_amp).



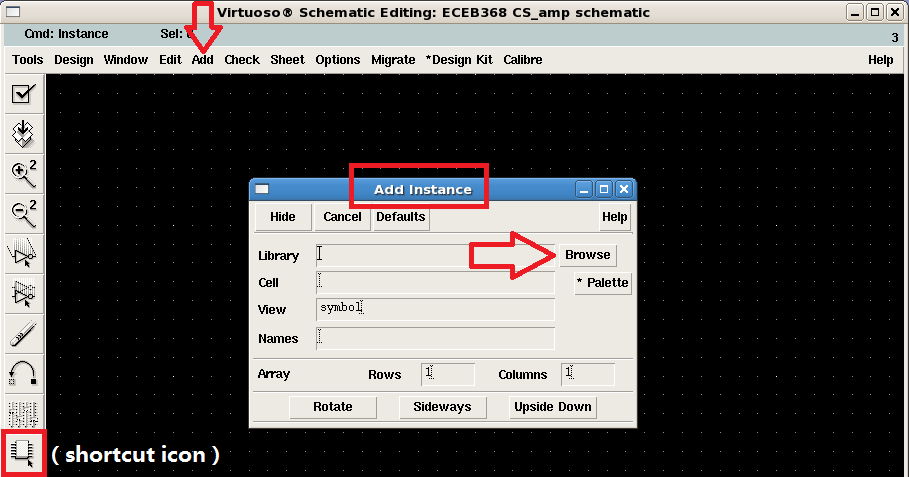
1. Press **OK** and the schematic window will appear.



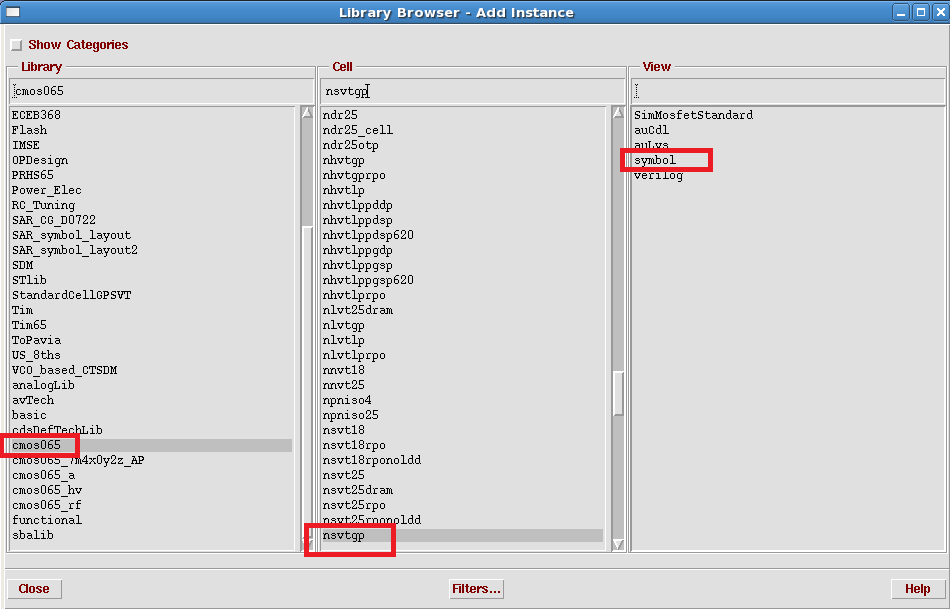
**IV. Add Components**

1. To add a MOSFET:

In the schematic view, choose **Add** -> **Instance** -> **Browse**



1. In the Library Browser window organized as “Library”, “Cell” and “View”, choose Library **cmos065** -> Cell **nsvtgp/psvtgp** for NMOS/PMOS (just an example here, in your project, please choose component type based on your own design requirement) -> View **symbol**.



*NOTE*: the meaning of the MOSFET name in STCMOS065 process:

**nsvtgp** -> **X Yvt Zp X**: the doping type of the active region, X=n means *N*MOS, X=p means *P*MOS.

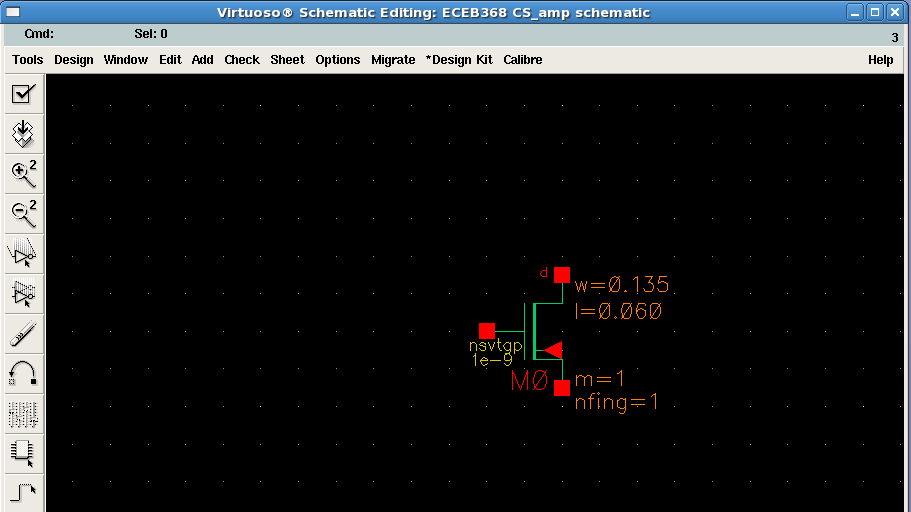
**Y**: the level of MOSFET’s threshold voltage (Vth), Y=s means *standard* Vth, Y=l means *low* Vth, Y=h means *high* Vth.

**Z**: the power level the MOSFET which is directly correlated to its drain current conduction. Z=g means *general* power, Z=l means *low* power. (**Hint**: for *lp* transistor, its transconductance is lower than *gp* type, which means its output impedance will be higher!)

For example: **nsvtgp** is standard Vth general power NMOS transistor.

Other types that maybe useful: *nsvtlp, nlvtgp, nlvtlp.*

1. In the schematic window, click on the mouse to place the component.



1. Press ESC to close the Add Instance window.

*NOTE*: You may press ESC to cancel the previously selected operation. You may also delete a component by pressing DELETE. There are also various shortcut icons that you may use and highlighted throughout this tutorial.

*NOTE*: To add other component (resistor/capacitor/sine-wave voltage source…)

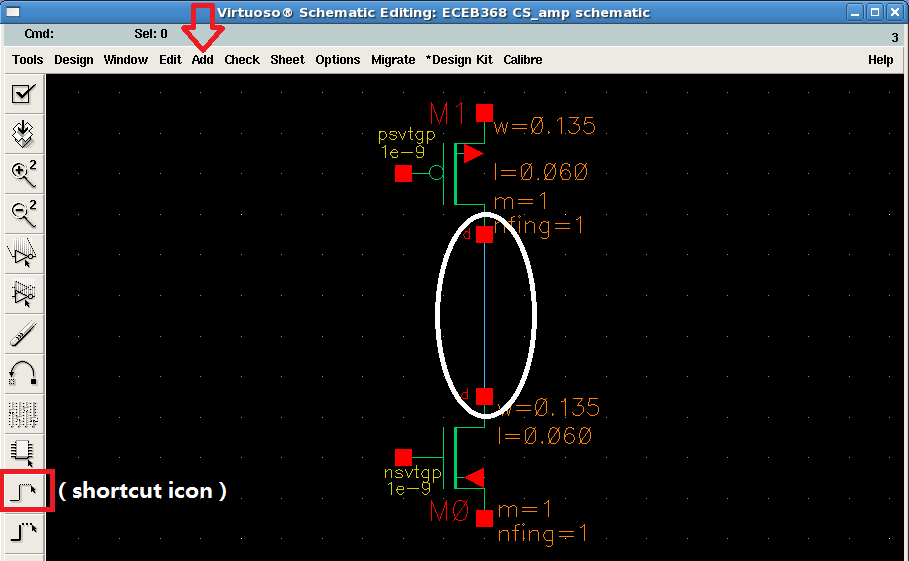
**Add** -> **Instance** -> **Browse**

Choose Library **analogLib** -> Cell **res/cap/vsin…** -> View **symbol**, then click to place the corresponding component.

1. You should now add all the components for a CS amplifier, i.e. 1 NMOS and 1 PMOS.

**V. Connect Components**

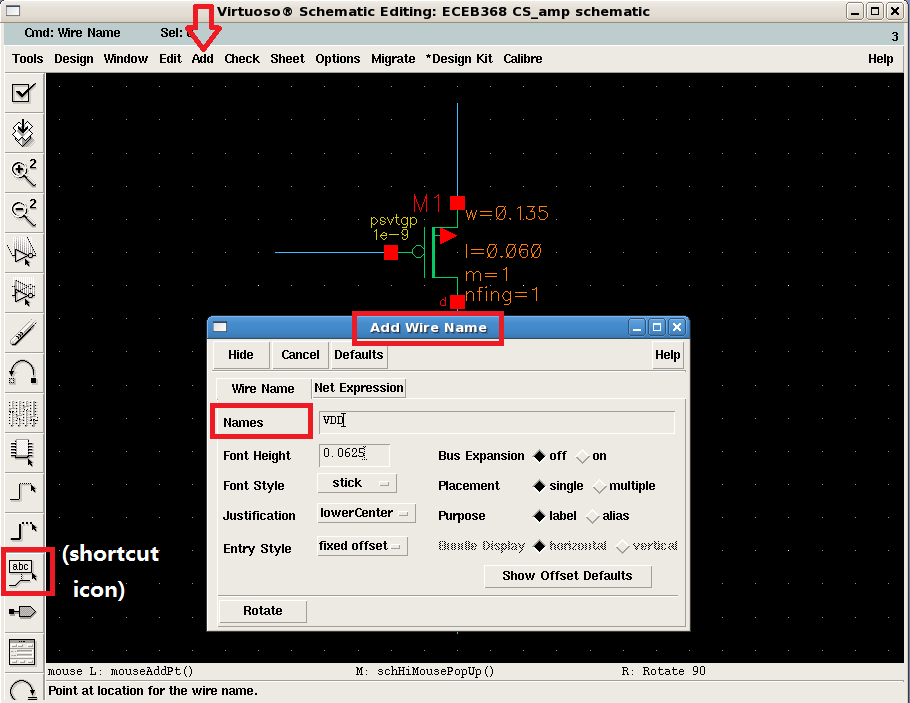
1. In the schematic view, choose **Add** -> **Wire (narrow)**
2. *Click* the terminal to be connected (e.g. D of the PMOS) -> *click* on the other terminal to be connected (e.g. D of the NMOS)



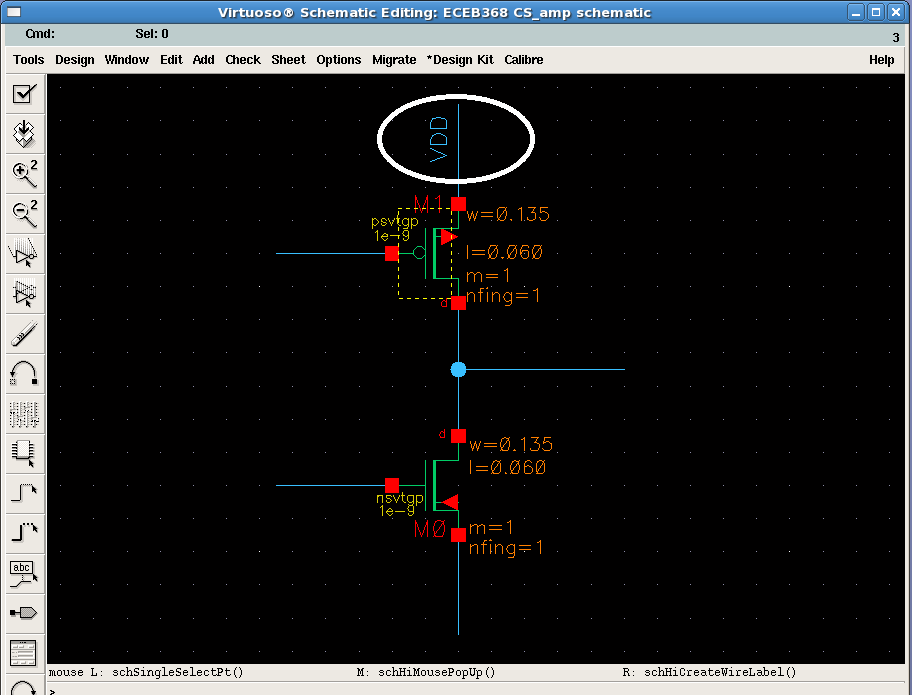
1. Finish the connection of the CS amp.

**VI. Add Wire Name**

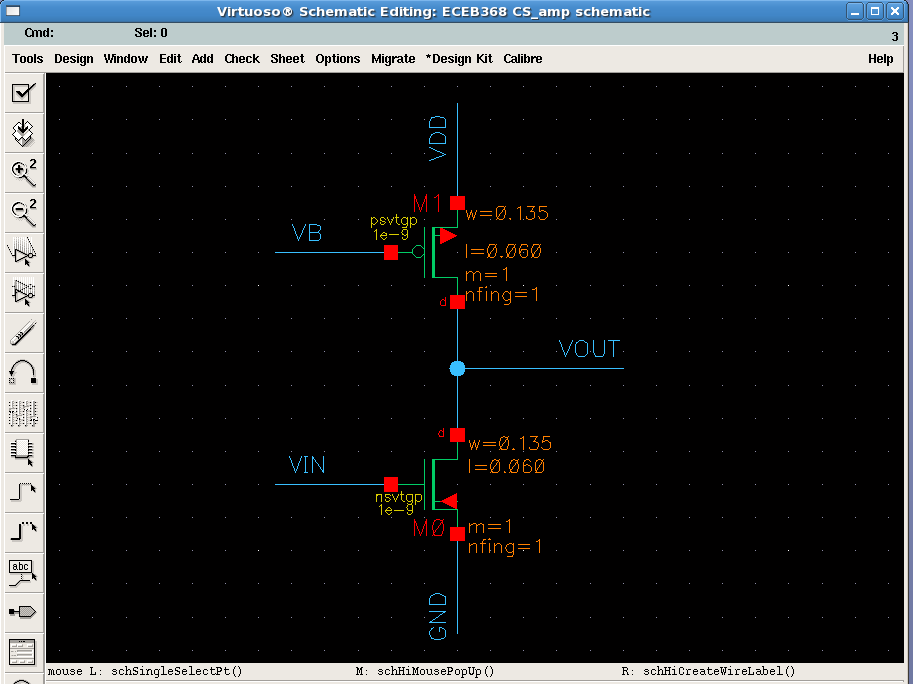
1. In the schematic view, choose **Add** -> **Wire Name**



1. Type the wire name in **Names** (e.g. VDD) -> choose **Hide**
2. *Exactly click* (with the small square on the wire) the wire that you want to name (e.g. the wire connected to the S of the PMOS).



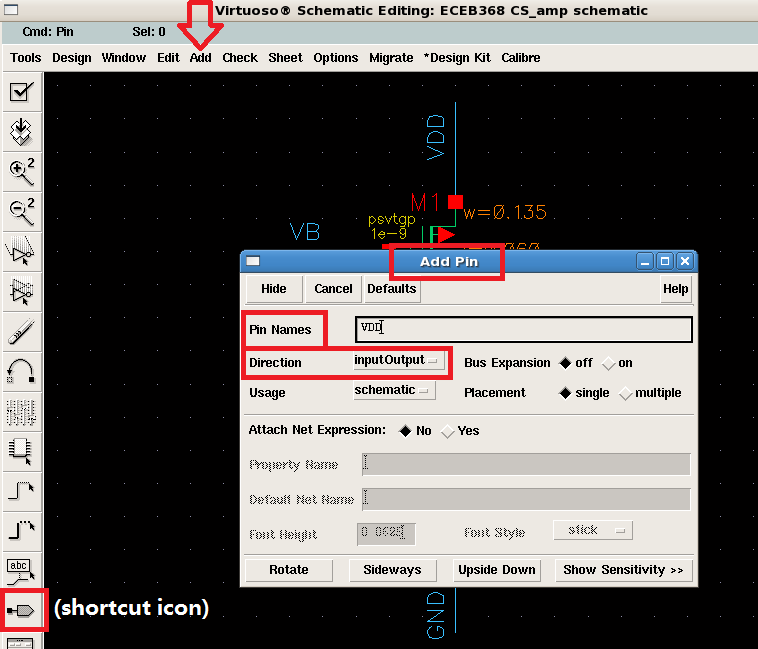
1. Finish naming all the nets that you think is needed (e.g. VDD, GND, VIN, VOUT and VB). (hint: you can type in multi-names in **Names** with space between each, and then respectively click the wires in the order of the typed names)



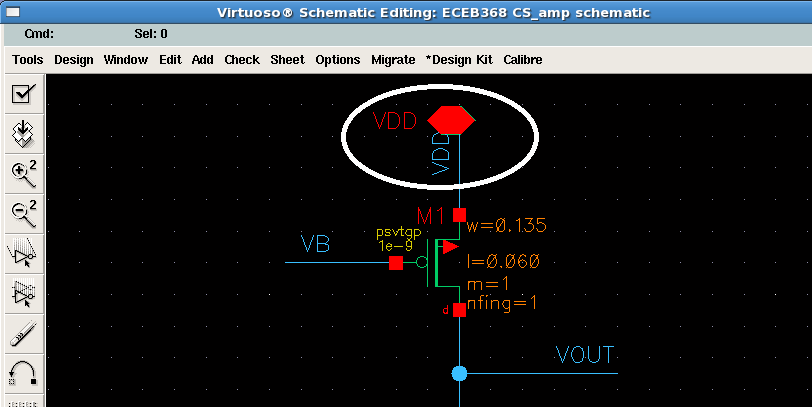
**VII. Add Pin**

The purpose of adding pin is for the use of creating a symbol for the designed circuit, which will be introduced in later section.

1. In the schematic view, choose **Add** -> **Pin**
2. Type the pin name in **Pin Names** (e.g. VDD) -> change the “**Direction**” from **input** to **inputOutput** -> press **Hide**

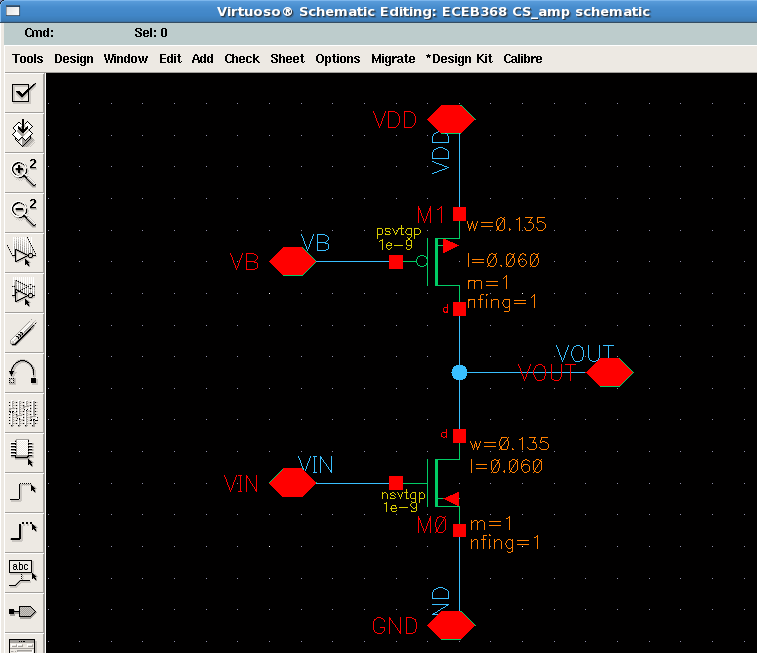


1. *Exactly click* (with the small square on the wire) the net that you want it as a pin (e.g. VDD).



1. Finish adding all the pins that is needed (e.g. VDD, GND, VIN, VOUT and VB). (hint: you can type in multi-names in **Names** with space between each, and then respectively click the nets in the order of the typed names)

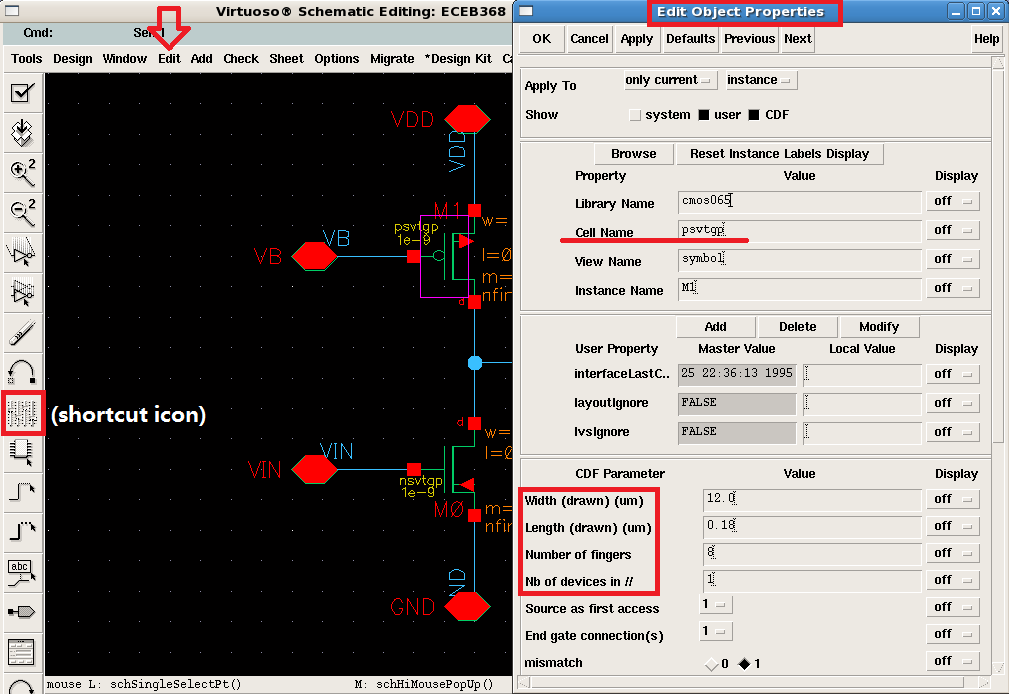
Note: you can also add pin to the wire that has not been named.



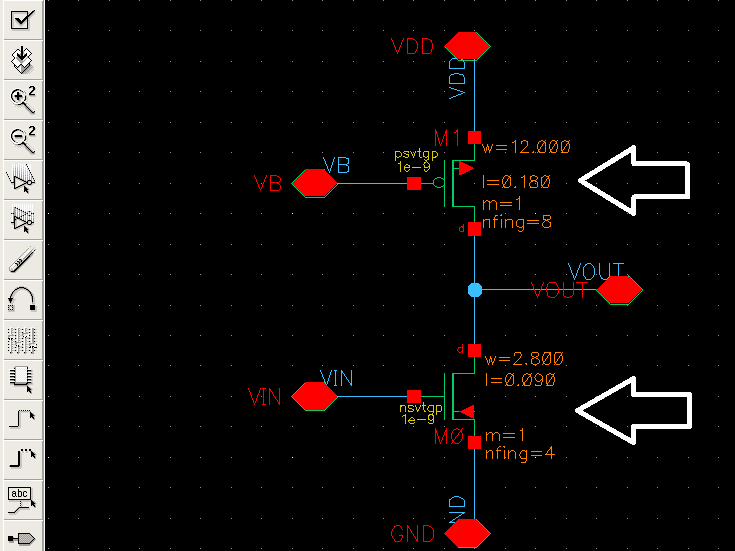
**VIII. Edit Component’s Properties**

The parameters of a component picked up from a library are preset as some default values. You need to edit them to fit your design requirements.

1. Click to *highlight* a component (e.g. the PMOS M1).
2. In the schematic view, choose **Edit** -> **Properties** -> **Objects**



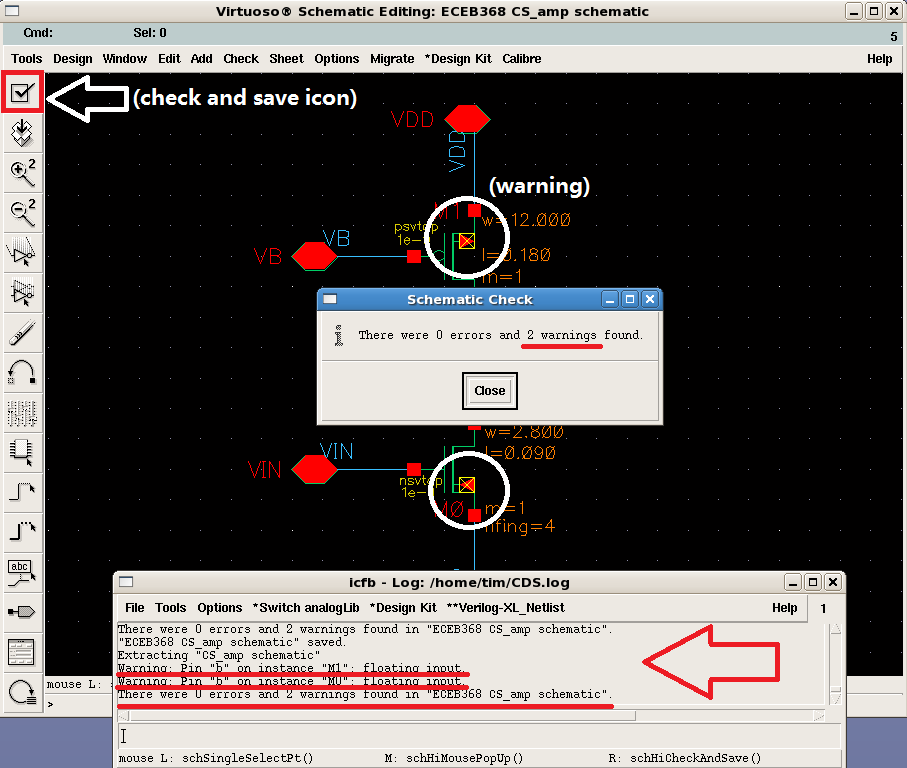
1. Edit the parameters that are needed in your design (e.g. **Width=**12 and **Length=**0.18, **Number of fingers=**8). (Careful about the unit of the edited parameters!) -> press **OK**.
2. Edit the properties of other components (e.g. the size of the NMOS M0: **Width=**2.8 and **Length=**0.09, **Number of fingers=**4).



**IX. Check and Save**

After finishing the construction of your circuit schematic, the cell view should be saved. (Note: it is highly recommended to do this operation frequently during your schematic entry process.)

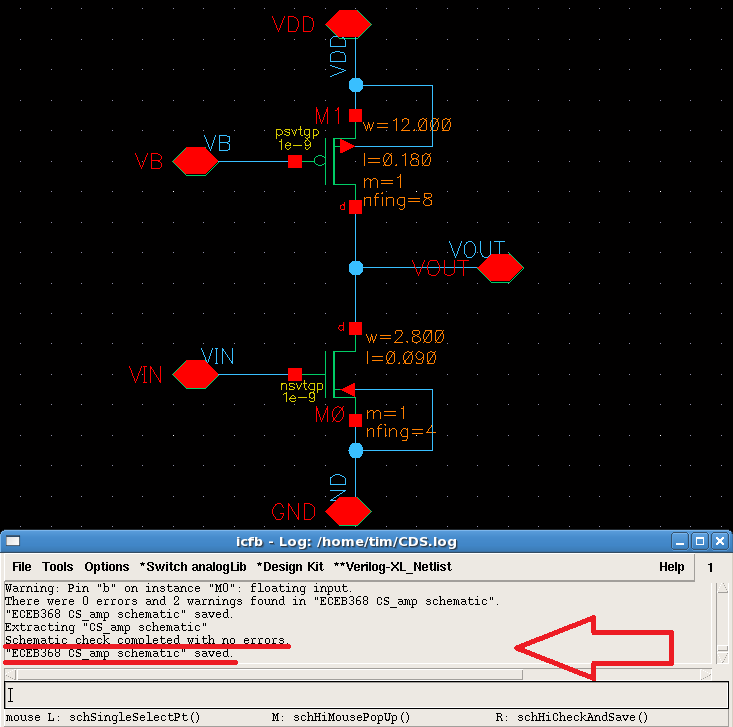
1. Choose the *shortcut icon* for **Check and Save** highlighted in the figure below.



1. You will see the number of *errors* and *warnings* found (e.g. 0 errors and 2 warnings) -> **Close** the message window.
2. The warnings will be highlighted in the schematic view, but errors will not. To check the details of the found errors and warning: see the *log* given in *icfb* window. (e.g. the body terminals of the NMOS and PMOS are not connected to a net.)

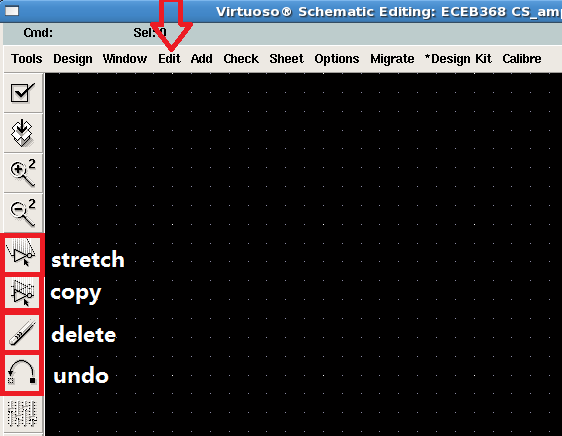
*NOTE:* 1) if you only **save** the file, Cadence will not check error and warning for you! 2) You cannot run simulation with error in the schematic, but you can run it with warning in.

1. By connecting the **b** of both MOSFET to VDD and GND, choose check and save again, the warnings should be removed.



**X. Some Useful Shortcut Icons and Hotkeys**

In spite of choosing different operations in pull-down menus and clicking on shortcut icons, there are various hotkeys that can be very useful, and can be found in the **Edit** list in the schematic view. Some frequently used shortcut icons are provided on the left hand side toolbar in the schematic window; some selected icons are highlighted as follows:



Using some hotkeys is very convenient in the schematic editing:

**i**: insert circuit elements

**w**: draw wire

**l**: add label

**p**: add pin

**q**: modify the properties of the selected element(s)

**c**: copy an element(s)

**shift+m**: move the selected element(s)

**right click+stretch a region+release**: zoom in a region

**f**: fit the window

**shift+x**: check and save

**u**: undo

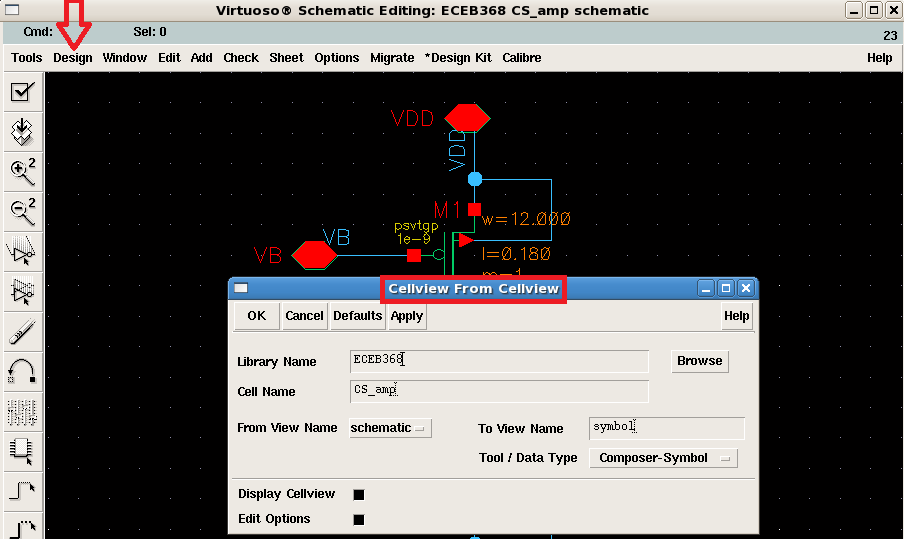
**Delete**: delete the selection

**ESC**: cancel the previous hotkey operation (hint: highly recommended to use frequently!)

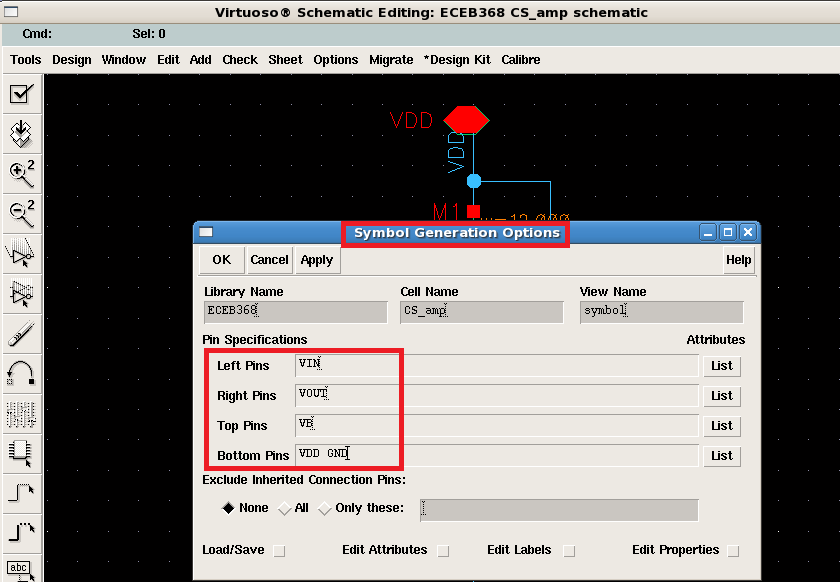
**XI. Create Symbol**

After finishing the construction of the circuit schematic, you may need a test-bench to test its performance. It is convenient to have a symbol to express the designed circuit in the test-bench.

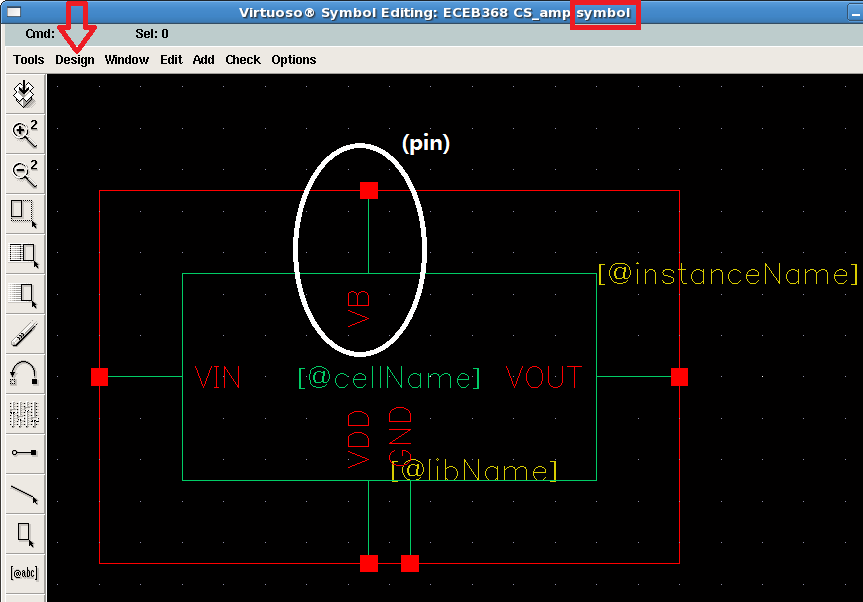
1. In the schematic view, choose **Design** -> **Create Cellview** -> **From Cellview**



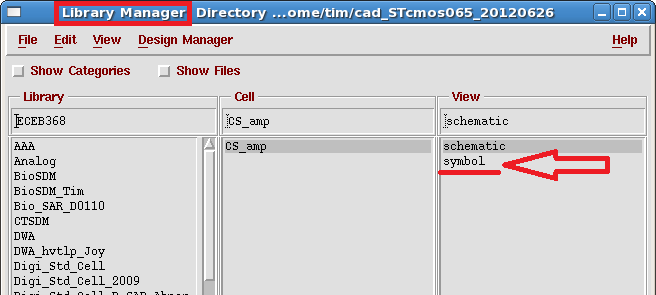
1. Choose **OK**.
2. In *Symbol Generation Options* window, rearrange the **Pin Specifications** (e.g. as shown in the figure below)



1. Choose **OK** you will see the symbol view. You can see many pins in the view, which are exactly the added pins in schematic view.
2. In the symbol view, choose **Design** -> **Check and Save**



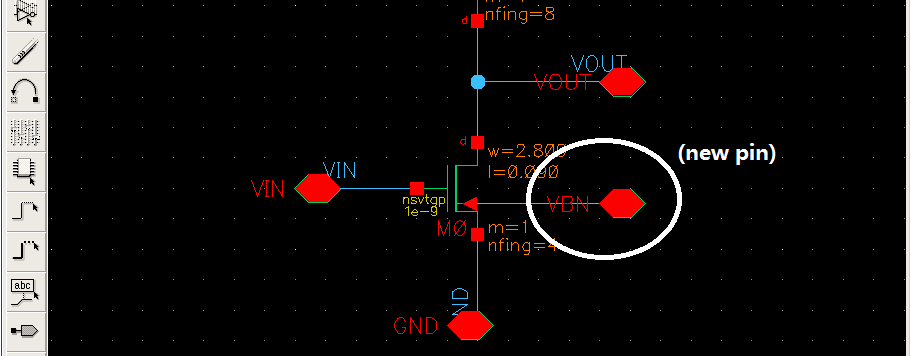
1. Then you can find a new generated *symbol* view in your library.



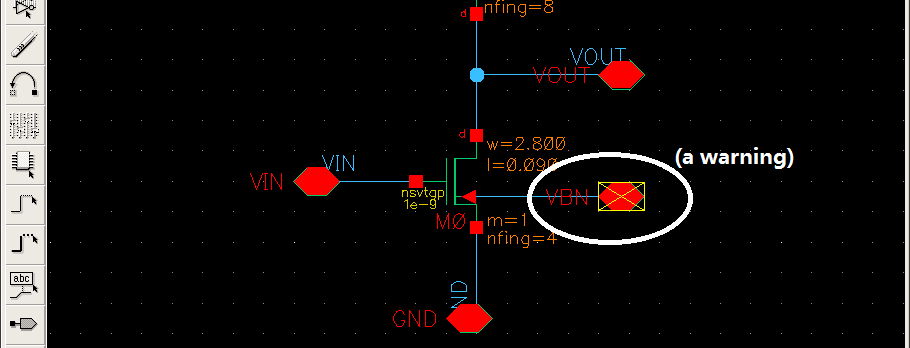
**XII. Update Symbol (FYI)**

After modifying the pins on the schematic, you should also update the corresponding pins in the symbol view.

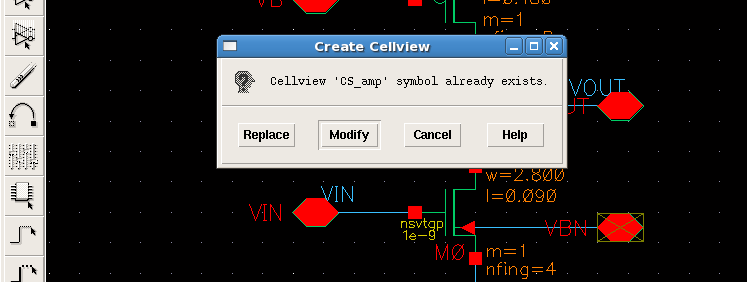
1. Edit pin in schematic view (e.g. add a new pin (VBN) to the bodyterminal of the NMOS M0).



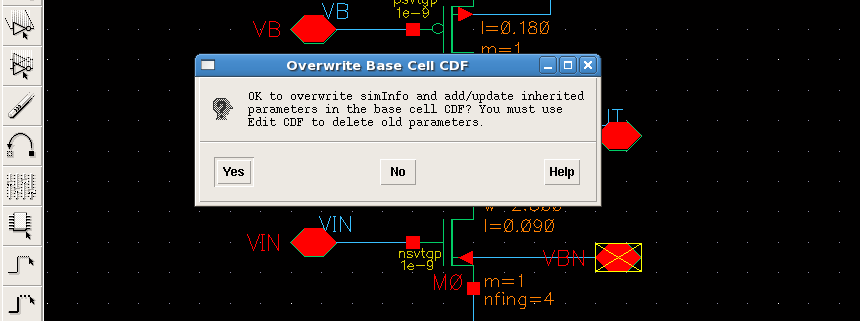
1. **Check and Save** the schematic, there will be a warning for the added pin.



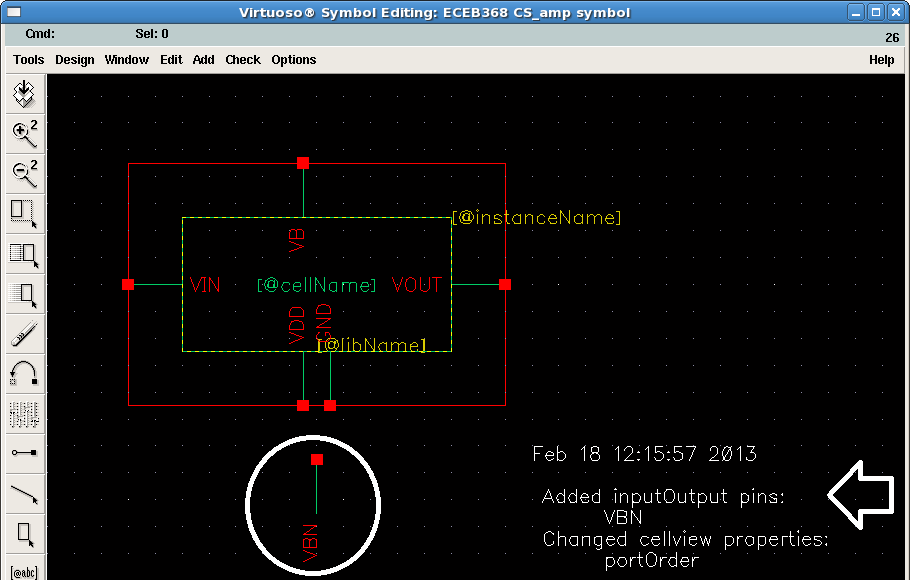
1. Repeat again the steps of creating a symbol: choose **Design** -> **Create Cellview** -> **From Cellview** -> **OK**, you will see the notice below.



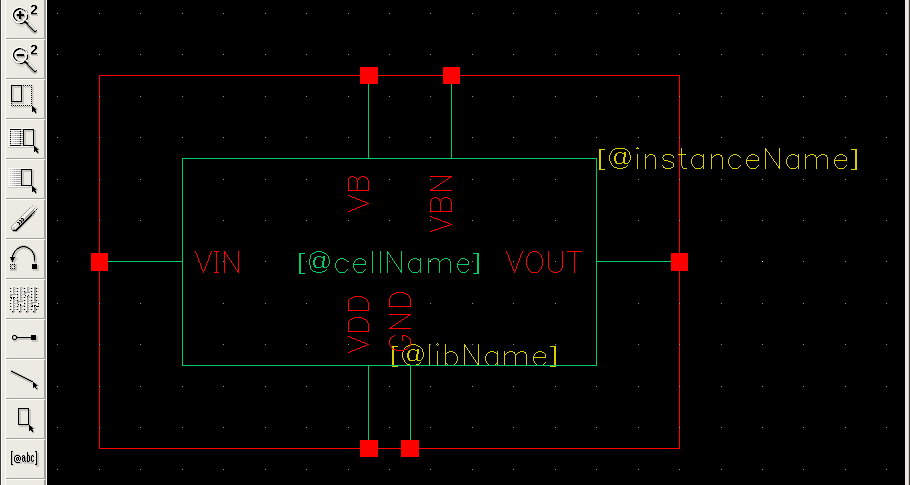
1. Choose **Modify**.



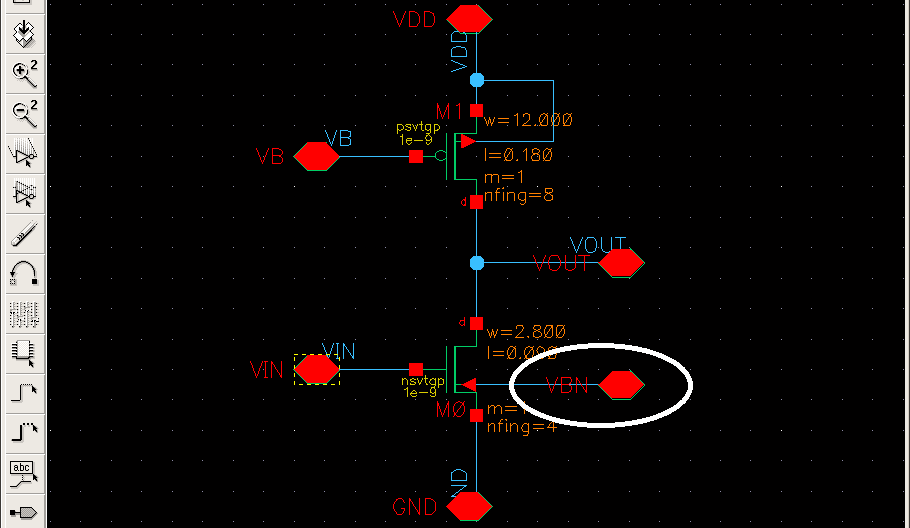
1. Choose **Yes**. Then you will see the added pin (VBN) is updated in the symbol view.



1. Delete the white texts and move the updated pin (VBN) to the position you like. Then **Check and Save** the symbol view.



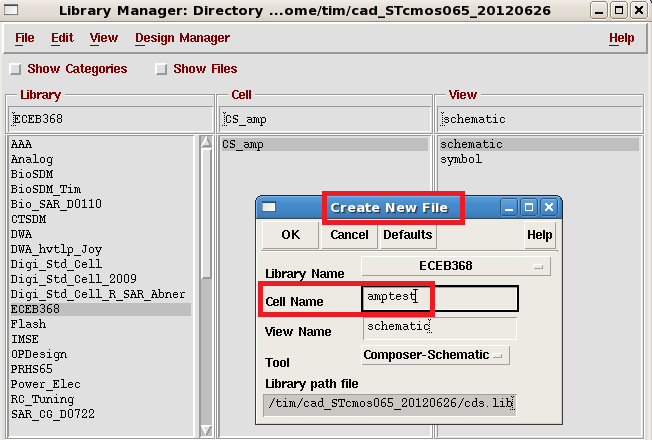
1. Back to the schematic view, **Check and Save** again then you will find that the previous warning for the added pin disappeared.



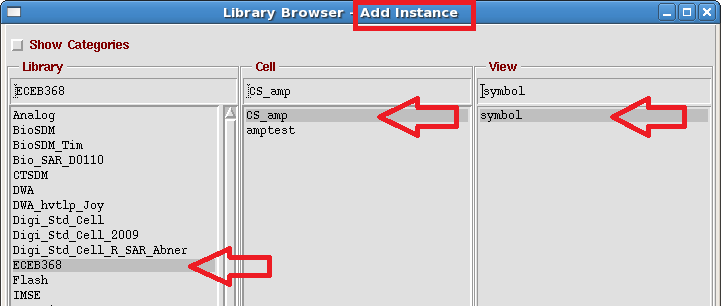
**XIII. Build Test-Bench**

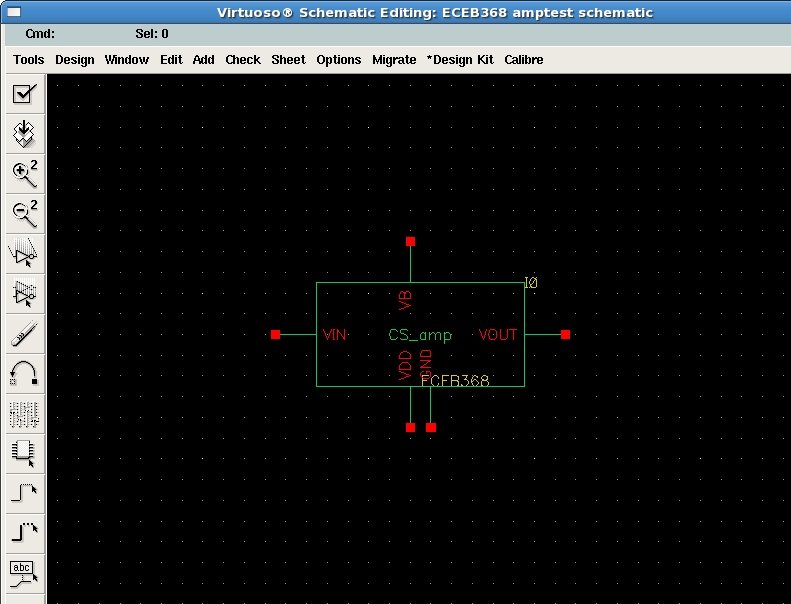
Test-bench is a platform for testing the performance of a designed building block. In general, different test-benches are required for verifying different performance parameters. In this project the design specification includes the small signal gain, GBW and static power consumption. We will build one test-bench to characterize these performances.

1. Create a new schematic cell (e.g. amptest) under your own created library (e.g. ECEB368) by the steps introduced in Section III.



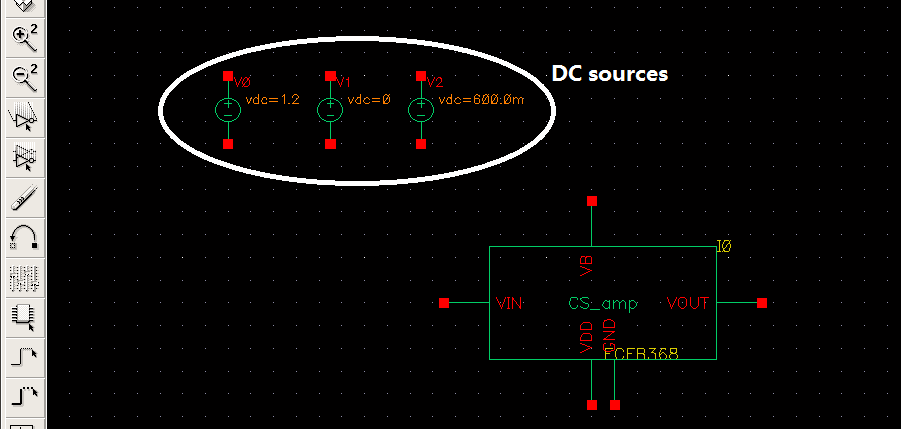
1. In the schematic view, pick up the designed CS amp from your own created library (by the steps introduced in Section IV): press ESC -> press hotkey **i** -> **Browse** -> choose Library (e.g. **ECEB368**) -> Cell **CS\_amp** -> View **symbol** -> click mouse to put down in schematic view.





1. Add DC supply and DC bias to the designed CS\_amp:
2. Add a dc voltage source (by the steps shown in Section IV): press ESC -> press hotkey **i** -> **Browse** -> Choose Library **analogLib** -> Cell **vdc** -> View **symbol** -> click mouse to put down.
3. Copy the added dc source: press ESC -> press hotkey **c** -> click the *vdc* source -> click an empty space.
4. Set the parameter for the *vdc* source: press ESC -> click to highlight the *vdc* -> press hotkey **q** -> change the *CDF Parameter* **DC voltage** into 1.2 (as VDD) (note: no need to type in unit).

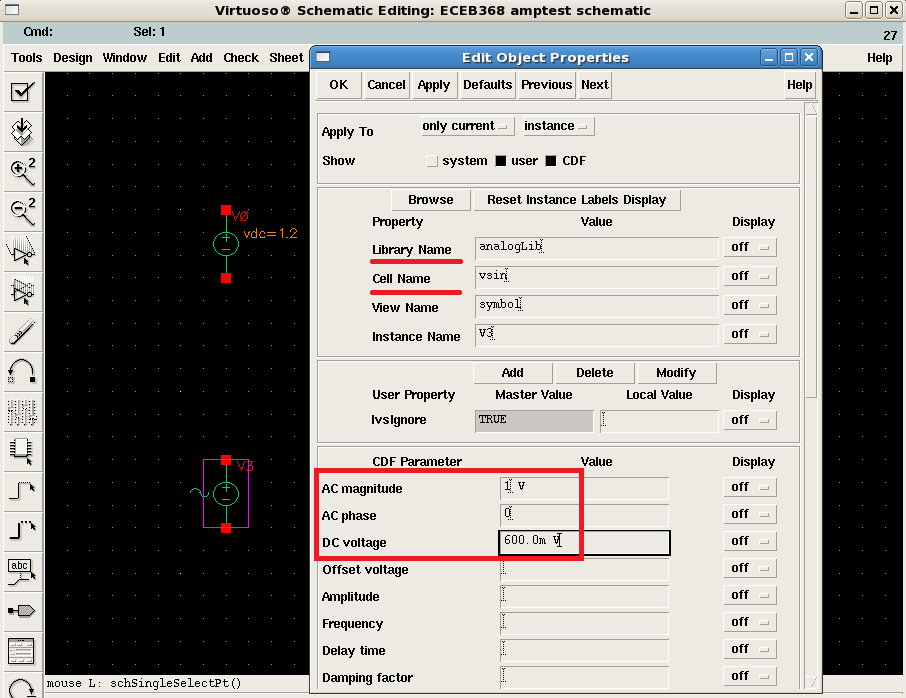
Follow the instructions above to finish the dc voltage source adding (1.2V for VDD, 0V for GND and 0.6V for VB).



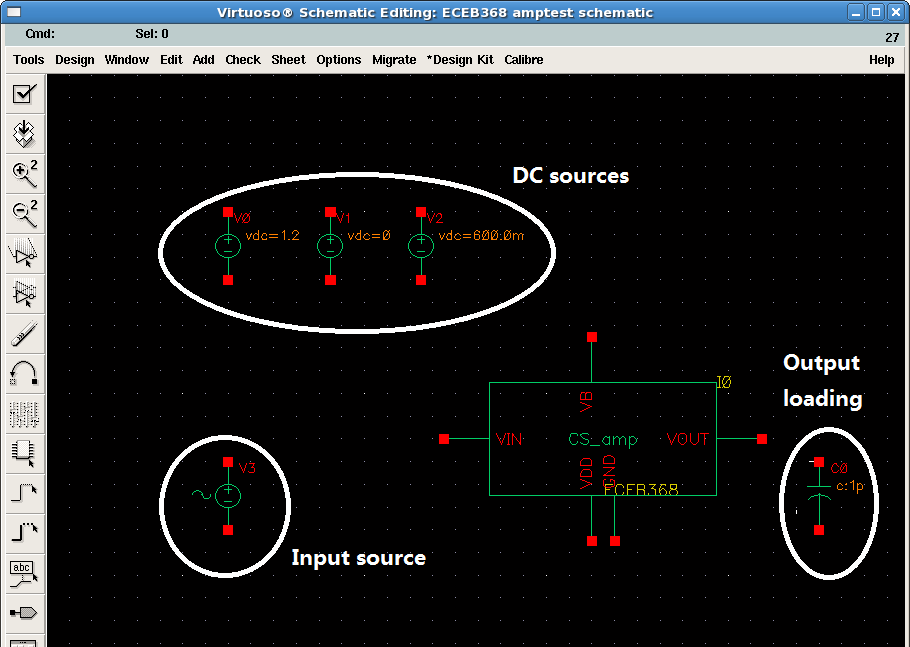
1. Add input source and output loading:

The input of the amp needs a DC bias; and we will test the small signal gain of the amp, so an AC test signal is also required at input. Hence the input signal contains both AC and DC components.

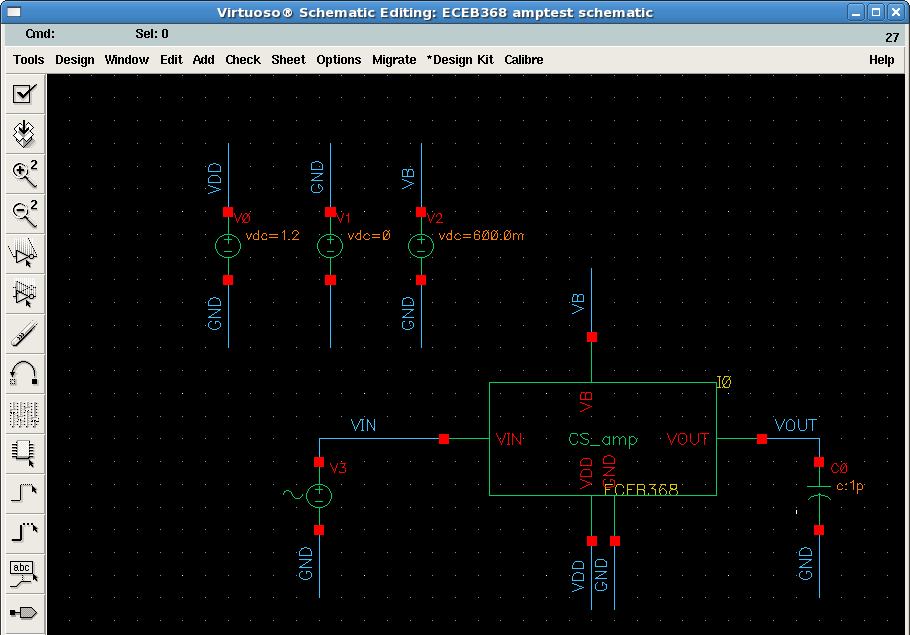
1. Add a *vsin* voltage source as input: press ESC -> press hotkey **i** -> **Browse** -> Choose Library **analogLib** -> Cell **vsin** -> View **symbol** -> click mouse to put down.
2. Set the parameters for *vsin*: press ESC -> click to highlight the *vsin* element -> press hotkey **q** -> set the *CDF Parameter* **AC magnitude** = 1 (as the AC test signal), **AC phase** = 0 and **DC voltage** = 0.6 (as the input DC bias) -> **OK**.



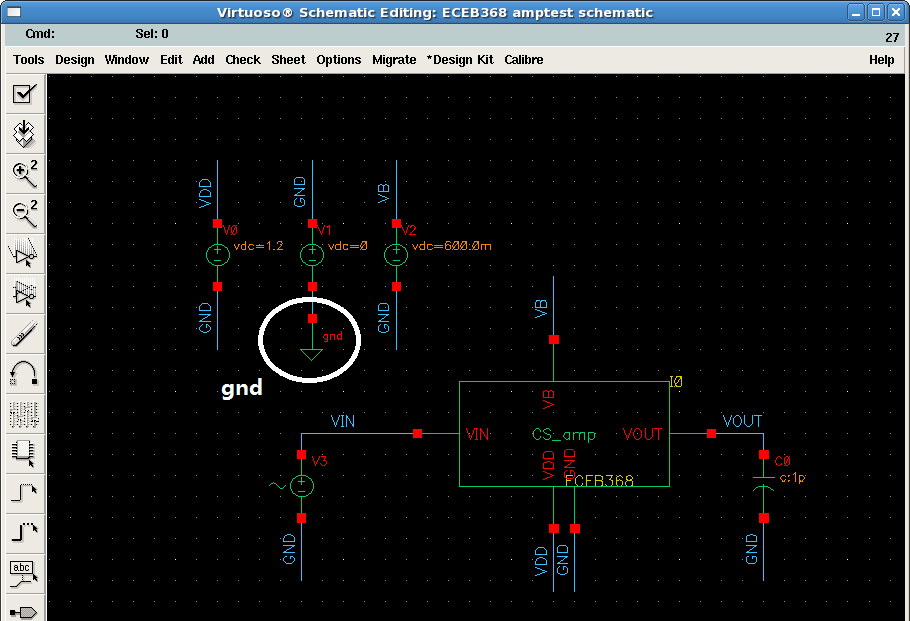
1. Add output capacitive loading: press ESC -> press hotkey **i** -> **Browse** -> Choose Library **analogLib** -> Cell **cap** -> View **symbol** -> click mouse to put down.
2. Set the CDF parameter **Capacitance** for *cap* as 1p (specification).



1. Connect the components and name the wires referring to the figure below. (Try to use the hotkey **w** and **l** to finish the operations.)



1. Add *gnd* terminal. The circuit needs a ground as the reference potential which we have not given yet. To give *gnd* terminal: press ESC -> press hotkey **i** -> **Browse** -> Choose Library **analogLib** -> Cell **gnd** -> View **symbol** -> connect it to the negative terminal of the GND DC source.

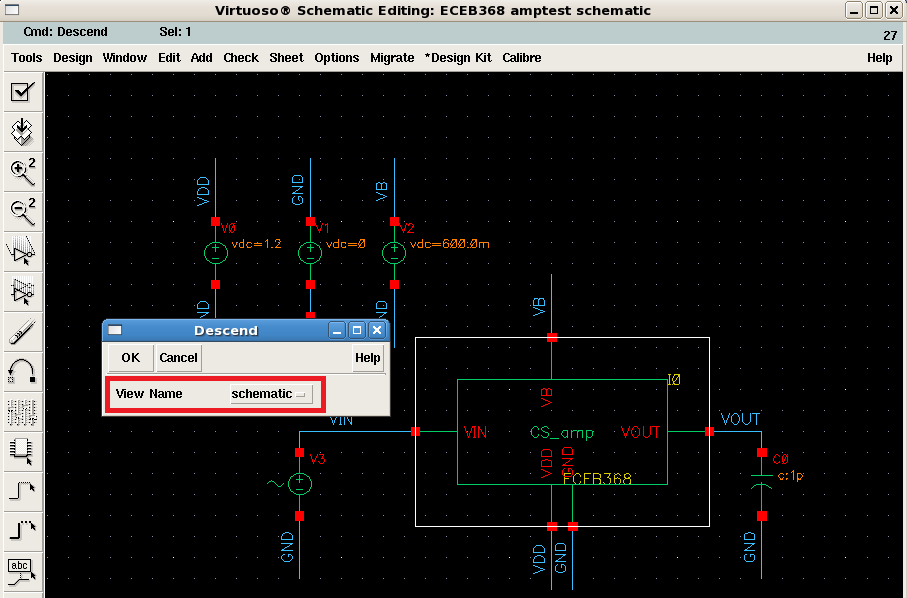


1. Check and save your schematic, make sure there is no error.

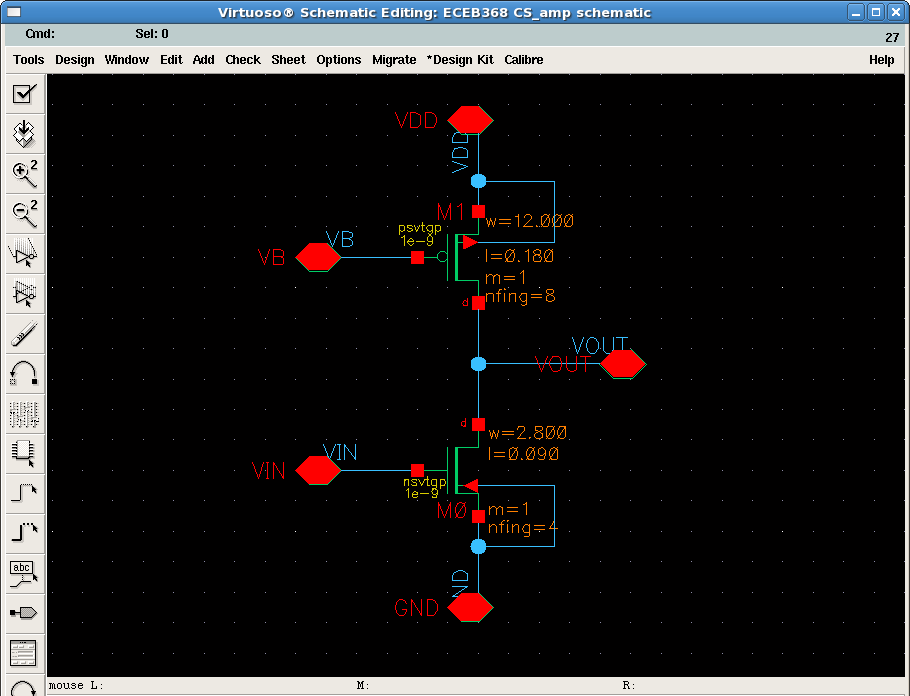
**XIV. Modify Schematic in Test-Bench**

You may find some issues and need to modify the designed schematic after you run it in the test-bench. It will be more convenient to achieve it by the following steps:

1. In the schematic view of your test-bench, click to highlight the cell that you are going to modify -> press **Shift + e**, you will see the following window.



1. Make sure the *View Name* is **schematic** -> Choose **OK**

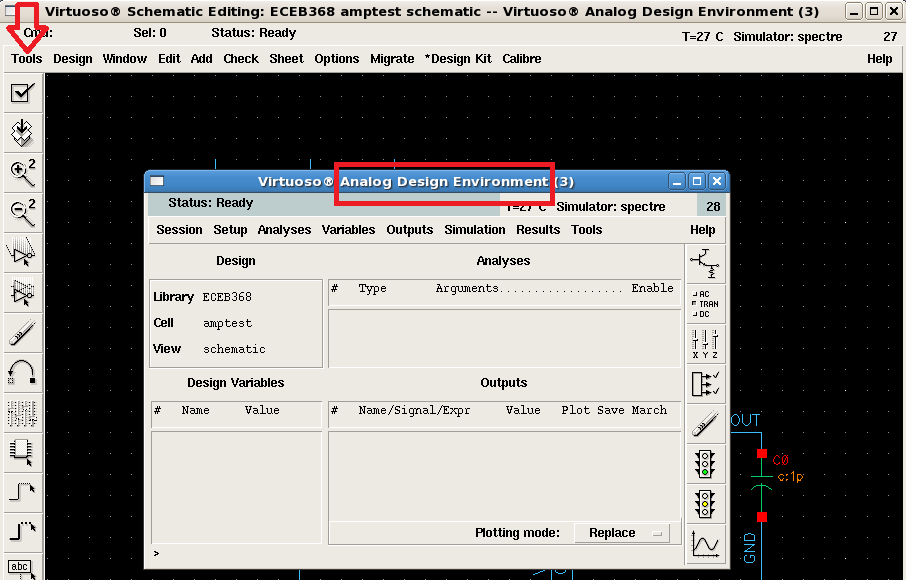


1. Modify the circuit schematic -> **Check and Save** -> press **Ctrl + e** to be back to the test-bench view -> **Check and Save** the test-bench.

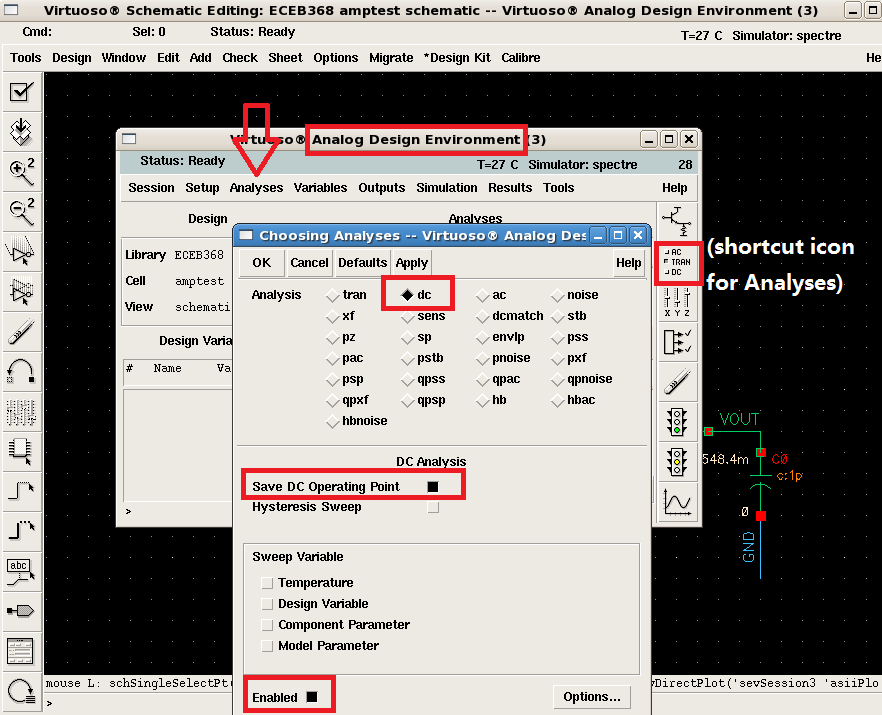
**XV. Run Simulation**

After finishing the construction of the test-bench, you can start to simulate the designed circuit. Both DC and AC analysis are necessary to characterize the large-signal and small-signal performance of the designed CS amp. Try to follow the following steps to setup your simulations.

1. In the schematic view, choose **Tools** -> **Analog Environment**

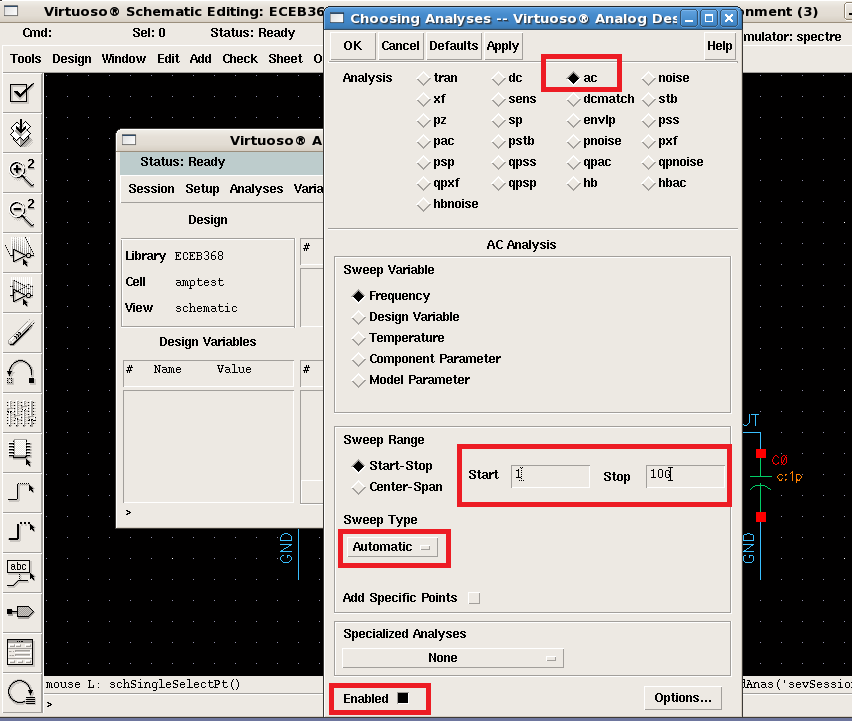


1. Setup DC analysis: in Analog Design Environment view, choose **Analyses** -> **Choose** -> choose **dc** -> select **Save DC Operating Point** -> make sure the **Enabled** on the left lower corner is selected.

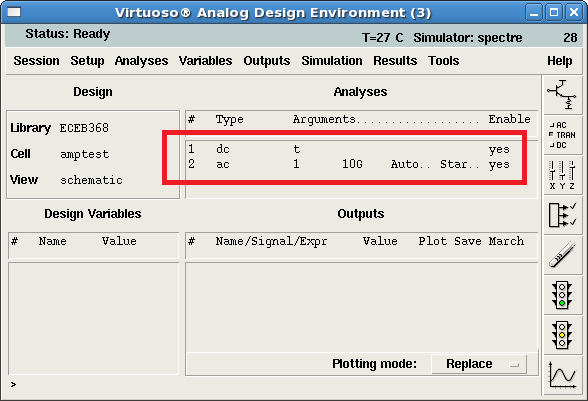


*NOTE:* If the **Save DC Operating Point** is not selected, Cadence will not save the DC operating points in the simulated result.

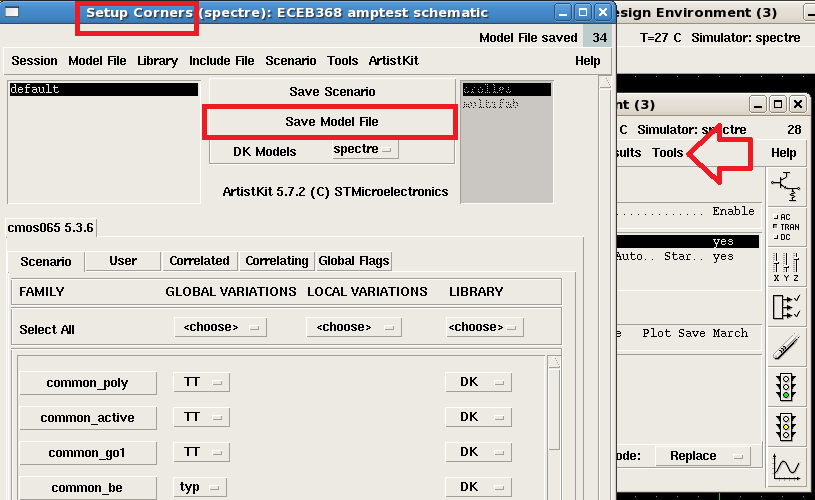
1. Set AC analysis: in the previous setting interface, choose **ac** -> in the *Sweep Range* bar, set **Start =** 1 and **Stop =** 10G (which is the swept frequency range in the analysis) -> set the *Sweep Type* as **Automatic** (you can choose linear or logarithmic type, but automatic is recommended in this project) -> make sure the **Enabled** on the left lower corner is selected.



1. Choose **OK**, you will see the analyses are attached in Analog Design Environment.

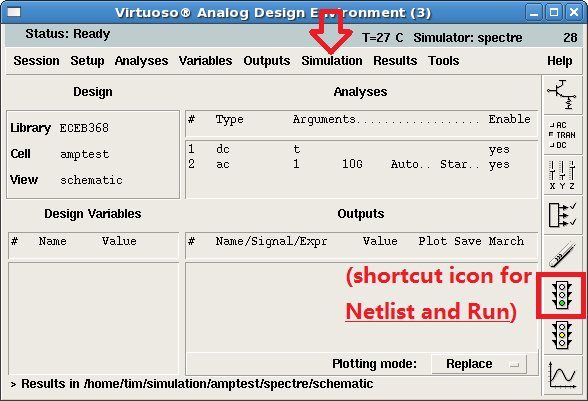


1. In Analog Design Environment view, choose **Tools** -> **Setup Corners ->** choose **Save Model File** -> close window.



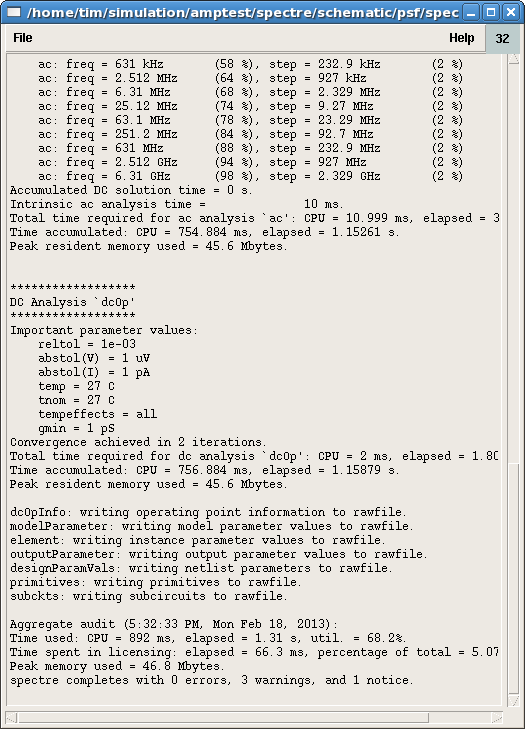
*NOTE:* if you forget to do this step, the model file will not be saved and you will not be able to run the simulation!

1. To run the simulation: in Analog Design Environment, choose **Simulation** -> **Netlist and Run**



*NOTE:* Netlist is the translated circuit description of schematic entry, and it should be generated before running a simulation. Spectre will perform the simulation based on the generated Netlist. If you choose **Run** to run the simulation, Cadence will not generate a new netlist based on the current schematic entry, which means the running simulation is based on the netlist generated last time. If the schematic is changed, the result will not be correct. So please run the simulation by choosing **Netlist and Run** if the schematic is updated.

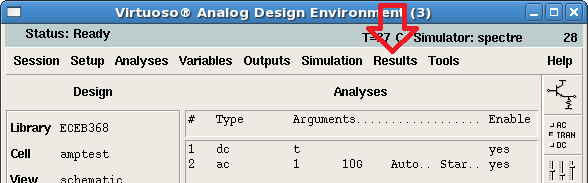
1. After the simulation, a log will be automatically shown. You can check and see if there are any errors/warnings.

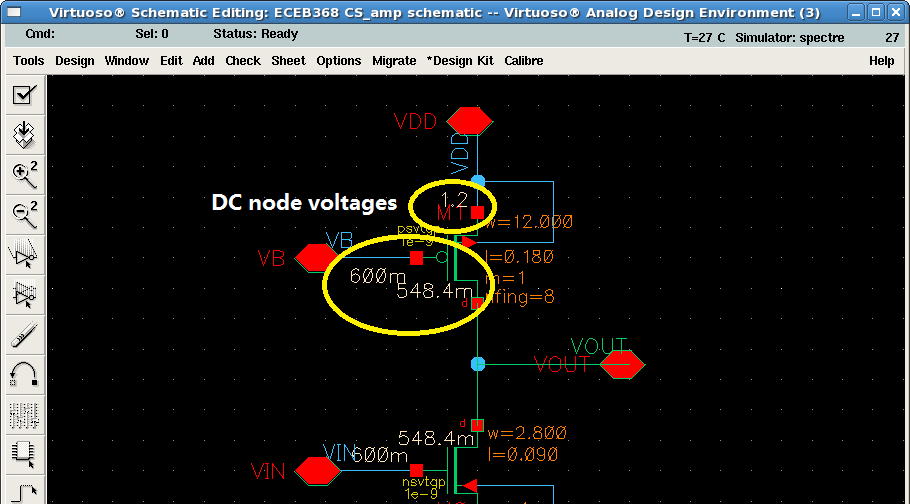


**XVI. Check Results**

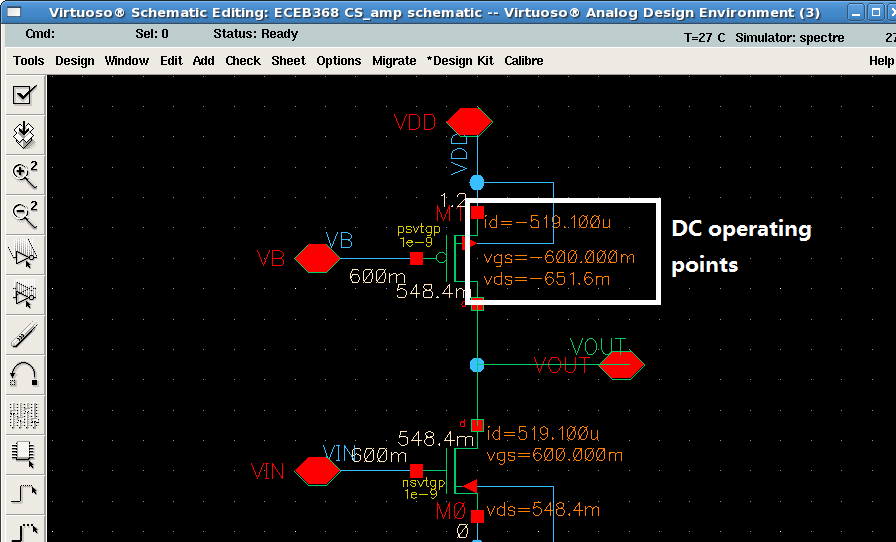
After finishing the simulation, you can follow the steps below to check the results.

1. Check the simulated results by DC analysis:
2. Since the schematic of the CS amp is not directly shown in the test-bench, to check its DC operating states, it is necessary to descend to the sub cell schematic view: click to highlight the CS­\_amp cell -> press **Shift + e**, *View Name* **schematic** -> **OK**
3. Display DC node voltage: in Analog Design Environment, choose **Results** -> **Annotate** -> **DC Node Voltage**



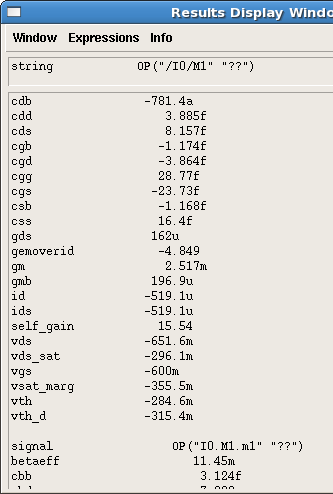


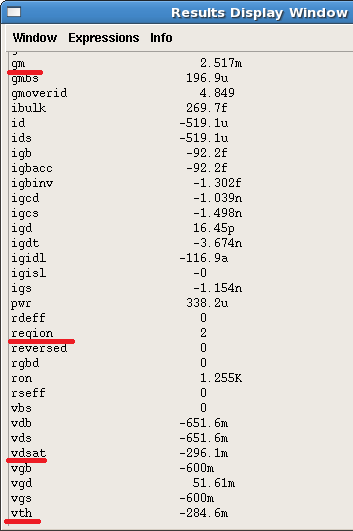
1. Display DC operating points for the MOSFET (i­D, vGS, vDS): choose **Results** -> **Annotate** -> **DC Operating Points**



*HINT:* the static power consumption can be calculated based on the simulated drain current.

1. Check the detailed DC operating points for a MOSFET: choose **Results** -> **Print** -> choose **DC Operating Points** -> in schematic view select the MOSFET (e.g. PMOS M1), a result list will be given (as below).

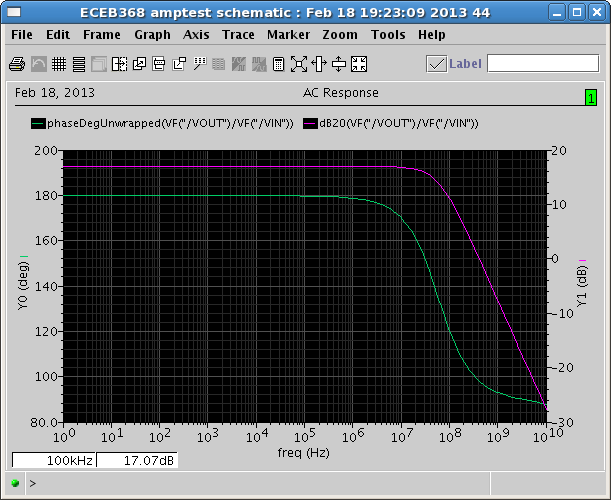




*HINT:* there are some important parameters you can check from the result above, such as **gm**, **vth**, **vdsat**, **region**, **gds**…

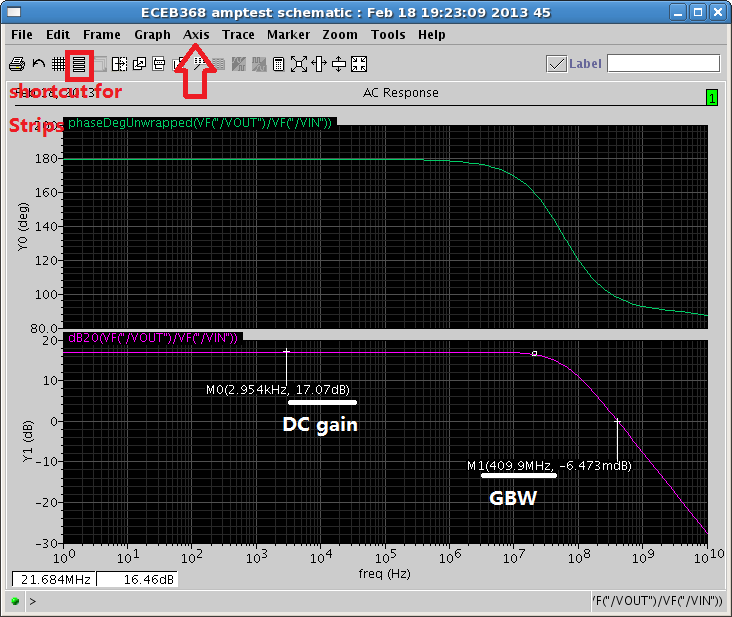
*NOTE:* **region** denotes the operating state of the transistor, **region** = 0/1/2/3 means the transistor is in cut off / triode / saturation / sub-threshold region respectively. Please also note that in cadence transistor is determined in saturation region for **vds > vdsat**; and if **vgs < vth**, the transistor will not directly operate in cut off region, but in sub-threshold region.

1. Check the simulated results by AC analysis:
2. There is no need to check AC result in sub cell schematic view, so you can choose to go back to the schematic view of the test-bench by pressing **Ctrl+e**.
3. Plot the frequency response of the CS amp: in Analog Design Environment, choose **Results** -> **Direct Plot** -> choose **AC Gain & Phase** -> in schematic view, select the output net *VOUT* -> then select the input net *VIN*.



There are two curves in the result, one is the magnitude of the frequency response which is also the small signal gain of the amp, and the other curve shows the phase which is related to the stability of the circuit.

1. The two curves can separately displayed by: choose **Axis** -> select **Strips**
2. To mark a data point on the curve: press hotkey **t** -> click the position you want to mark on the curve.

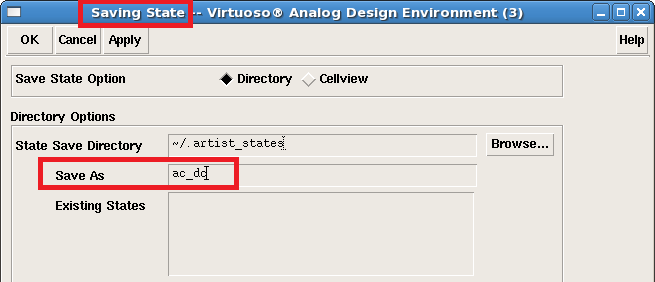


*HINT:* GBW can be considered equal to the unity gain frequency in this design.

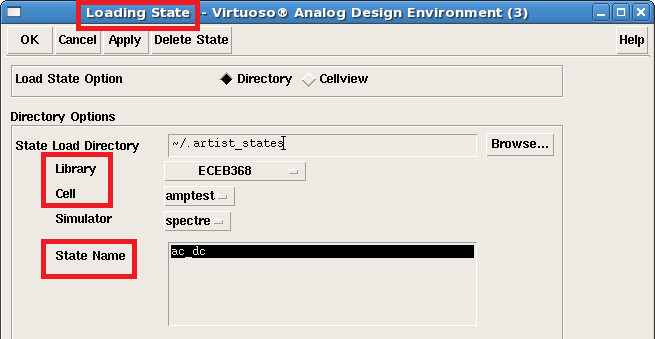
*NOTE:* the design example given in this tutorial does NOT meet the performance specification of your Project 1. You need to find your own ways to achieve the specifications.

**XVII. Exit Cadence**

1. Save the simulation setting: in Analog Design Environment, choose **Session** -> **Save State** -> name your saved state (e.g. ac­\_dc) in **Save As**.



1. If you need to load a saved state: in Analog Design Environment, choose **Session** -> **Load State** -> select the corresponding *Library*, *Cell* and *State Name* -> **OK**.



Note: even you load a saved simulation state; you still have to do the operation of saving the model file (Step XV. E), otherwise the simulation cannot be run.

1. When you need to exit Cadence, firstly close the Analog Design Environment window; close the icfb in the last step.

**XVII. Appendix**

Instead of the using the icons, you can also try out the following hot-keys to perform specific tasks when you draw your schematic:

|  |
| --- |
| **X:** check and save |
| **f:** fit the window |
| **z:** zoom |
| **u:** undo |
| **m:** stretch |
| **c:** copy |
| **M:** move the selected element(s) |
| **del:** delete |
| **q:** object property |
| **i:** instance |
| **l:** add label |
| **w:** wire |
| **p:** pin |
| **z:** zoom in |

**End of Tutorial 1a**